

WHAT IS CLAIMED IS:

1 1. An apparatus for controlling a physical layer interface
2 of a network interface card in real time, said apparatus
3 comprising:

4 a first memory capable of storing a multitasking control
5 program, said multitasking control program comprising a main
6 routine and a plurality of subroutines callable by said main
7 routine;

8 a second memory capable of storing a plurality of
9 multitasking vectors associated with said multitasking control
10 program; and

11 a microcontroller capable of executing said multitasking
12 control program,

13 wherein program execution control is transferred from
14 said main routine to a first one of said plurality of subroutines
15 when said first subroutine is called by said main routine and
16 wherein said first subroutine, upon encountering a decision point
17 in said first subroutine that is not yet capable of being decided,
18 updates a first one of said plurality of multitasking vectors
19 associated with said first subroutine with an address of said
20 decision point and transfers program execution control back to said
21 main routine.

1 2. The apparatus as set forth in Claim 1 wherein said main
2 routine uses said first multitasking vector to subsequently
3 transfer program execution control back to said first subroutine at
4 said address of said first decision point.

1 3. The apparatus as set forth in Claim 2 wherein said first
2 memory comprises a read-only memory (ROM) associated with said
3 microcontroller.

1 4. The apparatus as set forth in Claim 3 wherein said second
2 memory comprises a random access memory (RAM) associated with said
3 microcontroller.

1 5. The apparatus as set forth in Claim 4 wherein said ROM
2 and said RAM are internal to said microcontroller.

1 6. The apparatus as set forth in Claim 4 wherein at least
2 one of said ROM and said RAM comprises an external device coupled
3 to said microcontroller.

1 7. The apparatus as set forth in Claim 2 wherein said first
2 memory and said second memory comprise a random access memory (RAM)
3 associated with said microcontroller.

1 8. The apparatus as set forth in Claim 7 wherein said RAM
2 comprises an external device coupled to said microcontroller.

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1 9. A processing system comprising:
2 a data processor;
3 a network interface card for coupling said processing
4 system to a data network, said network interface card comprising an
5 apparatus for controlling a physical layer interface of said
6 network interface card in real time, said apparatus comprising:
7 a first memory capable of storing a multitasking
8 control program, said multitasking control program comprising
9 a main routine and a plurality of subroutines callable by said
10 main routine;
11 a second memory capable of storing a plurality of
12 multitasking vectors associated with said multitasking control
13 program; and
14 a microcontroller capable of executing said
15 multitasking control program,
16 wherein program execution control is transferred
17 from said main routine to a first one of said plurality of
18 subroutines when said first subroutine is called by said main
19 routine and wherein said first subroutine, upon encountering
20 a decision point in said first subroutine that is not yet
21 capable of being decided, updates a first one of said
22 plurality of multitasking vectors associated with said first

23 subroutine with an address of said decision point and
24 transfers program execution control back to said main routine.

1 10. The processing system as set forth in Claim 9 wherein
2 said main routine uses said first multitasking vector to
3 subsequently transfer program execution control back to said first
4 subroutine at said address of said first decision point.

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1 14. The processing system as set forth in Claim 12 wherein at
2 least one of said ROM and said RAM comprises an external device
3 coupled to said microcontroller.

1 15. The processing system as set forth in Claim 10 wherein
2 said first memory and said second memory comprise a random access
3 memory (RAM) associated with said microcontroller.

1 16. The processing system as set forth in Claim 15 wherein
2 said RAM comprises an external device coupled to said
3 microcontroller.

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1 17. For use in a network interface card having a physical
2 layer interface controllable by a microcontroller embedded therein,
3 a method of operating the microcontroller comprising the steps of:

4 storing a multitasking control program, the multitasking
5 control program comprising a main routine and a plurality of
6 subroutines callable by the main routine;

7 storing a plurality of multitasking vectors associated
8 with the multitasking control program; and

9 executing the multitasking control program in s
10 microcontroller;

11 transferring program execution control from the main
12 routine to a first one of the plurality of subroutines when the
13 first subroutine is called by the main routine;

14 when the first subroutine encounters a decision point in
15 the first subroutine that is not yet capable of being decided,
16 updating a first one of the plurality of multitasking vectors
17 associated with the first subroutine with an address of the
18 decision point; and

19 transferring program execution control back to the main
20 routine.

1 18. The method as set forth in Claim 17 further comprising
2 the step of using the first multitasking vector to subsequently
3 transfer program execution control from the main routine back to
4 the first subroutine at the address of the first decision point.

1 19. The method as set forth in Claim 18 wherein the first
2 memory comprises a read-only memory (ROM) associated with the
3 microcontroller.

1 20. The method as set forth in Claim 19 wherein the second
2 memory comprises a random access memory (RAM) associated with the
3 microcontroller.

1 21. The method as set forth in Claim 20 wherein the ROM and
2 the RAM are internal to the microcontroller.

1 22. The method as set forth in Claim 20 wherein at least one
2 of the ROM and the RAM comprises an external device coupled to the
3 microcontroller.